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Attorney for Applicant

PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Henry Esmond Butterworth	
Serial No.:	10/080,488	Group Art Unit: 2188
Filed:	02/22/2002	
For:	LOG-STRUCTURE ARRAY	
Examiner:	Reginald Glenwood Bragdon	

APPELLANT'S AMENDED APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

On July 13, 2004, Appellant filed a timely Notice of Appeal from the Final Office Action mailed April 13, 2004. Appellant appeals from the rejection of all pending claims.

This Brief is being filed under the provisions of 37 C.F.R. § 41.37. The filing fee set forth in 37 C.F.R. § 41.20(b)(2) of Three Hundred and Forty Dollars ($340.00) was previously submitted with the Appeal Brief filed on July 13, 2004. The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or to credit any overpayment, to Deposit Account No. 09-0466.

1. REAL PARTY IN INTEREST

The real party in interest is the assignee, International Business Machines Corporation, Armonk, New York.

2. RELATED APPEALS AND INTERFERENCES

There are no related appeals and interferences.

3. STATUS OF CLAIMS

Claims 1-22 stand rejected under 35 U.S.C. §§ 112 and 103. Specifically, the Final Office Action, mailed April 13, 2004, rejected Claim 11 under 35 U.S.C. §112, first paragraph for failing to comply with the written description requirement. Claims 1-8, and 12-22 stand rejected under 35 U.S.C. §103(a) as obvious in view of U.S. Patent No. 6,058,489 to Schultz et al. (hereinafter "Schultz") and U.S. Patent No. 5,671,390 to Brady et al. (hereinafter "Brady"). Claims 1-22 stand rejected under 35 U.S.C. §103(a) as obvious in view of U.S. Patent No. 5,758,118 to Choy et al. (hereinafter "Choy") and Brady. Claims 1-22 are pending and are hereby appealed.

4. STATUS OF AMENDMENTS

Appellant filed an Amendment July 19, 2004 to place the claims in better condition for appeal. An Advisory Action mailed August 16, 2004 indicated that the amendments have not been entered. The Advisory Action did indicate that the Claim 11 rejection can be overcome with the amendment proposed to that claim. Pending a decision on the appealed claims, Appellant is prepared to resubmit the acceptable proposed amendment to Claim 11. The Examiner asserted that the amendments would require further search and consideration and do not materially reduce or simplify the issues for appeal.

5. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1

Claim 1 defines a processor 102 connected to an information storage system 104 having N+1 storage devices 106 in which information is maintained as a Log Structured Array (LSA) by

way of a control unit 108. *See* Figure 1, Specification page 11, lines 4-8, lines 24-26 and page 7, lines 5-10. The control unit 108 includes a controller 112 that communicates with a LSA directory 116 to implement an LSA controller 112. *See* Figure 1, Specification page 12, lines 19-26.

The storage devices 106 store the information in stripes that extend across the storage devices. *See* Figure 1, Specification, page 7, lines 5-10. Each stripe is further divided into strips (D0, D1, D2, etc) which store a whole number of logical tracks. *See* Specification, page 7, lines 5-10, Figure 2. Each stripe may include a parity strip and a certain number of data strips. *Id.*

The LSA directory 116 manages the locations and storage of the tracks stored in the array (plurality of storage devices). *See* Specification, page 7, lines 10-15. The LSA directory 116 maintains the location of each logical track by storing the stripe number for the logical track and an offset of the logical track within the stripe. *See* Specification, page 16, lines 16-18, page 7, lines 10-18. This type of addressing is used instead of logical block addressing (LBA). *See* Specification, page 16, lines 16-18. Addressing logical tracks using a stripe number and an offset is a form of addressing (explained below) well known in the art as relative addressing which is specifically referenced in Claim 1.

Claim 1 further defines connecting an additional storage device (Disk 4) to the LSA controller 112 by adding the storage device as a member of the RAID array 106. *See* Specification, page 18, lines 1-3, Figures 1 and 3. Claim 1 then logically appends an additional strip to each stripe in the LSA directory 116. *See* Specification, Figure 3, page 20, lines 17-19, page 7, lines 14-18, page 8, lines 5-9. Logically appending an additional strip would not be possible if addresses in the LSA directory 116 were based on logical block addresses. *See* Specification, page 20, lines 21-26.

Typically, appending an additional strip involves adding an entry to the directory 116 for each new strip. Advantageously, the storage device is appended without moving any existing strips or optionally moving a minimal number of strips. *See* Specification, page 8, lines 24-27. The relative addressing used in the LSA directory allows the addition of a storage device without affecting the addresses of other logical tracks indexed within the directory.

Claim 12

Claim 12 defines substantially the same subject matter as Claim 1 in the form of an apparatus claim directed toward the LSA controller 112 as opposed to a method claim. The LSA controller, logic device, information processing system, processor, plurality of information storage devices, additional storage device, stripes, new strip, directory, and relative addresses substantially correspond to like named elements recited in Claim 1.

Claim 16

Claim 16 defines substantially the same subject matter as Claim 1 in the form of an apparatus claim directed toward the LSA controller 112 as opposed to a method claim. The LSA controller, logic device, information processing system, processor, plurality of information storage devices, additional storage device, stripes, new strip, directory, and relative addresses substantially correspond to like named elements recited in Claim 1.

Additionally, Claim 16 defines a means for connecting the additional information storage devices to the LSA controller. This means may comprise a variety of structures including adding the storage device as a member of the RAID array 106. *See* Specification, page 18, lines 1-3, Figures 1 and 3. Those of skill in the art readily recognize that this may include physically coupling an additional storage device (Disk 4) to the read data path 120 and write data path 130. *See* Specification, page 13, lines 2-11. In addition, adding a storage device to a RAID array 106 may also include registering the presence of the storage device with a RAID controller such as controller 112 through a configuration change.

Claim 16 also defines a means for logically appending an additional strip to the end of each stripe in the directory 116. Such means are taught in the form of the added column illustrated in the tabular representation of the RAID 5 array. *See* Specification, Figures 3 and 4, page 17, lines 1-3, page 20, lines 17-19, page 7, lines 14-18, page 8, lines 5-9. The tabular representation is a logical representation of the organization of tracks and addressing of tracks within the LSA directory 116.

Claim 20

Claim 20 defines substantially the same subject matter as Claim 1 in the form of a system claim directed toward an information storage system as opposed to a method claim. The LSA controller, information processing system, processor, plurality of information storage devices, additional storage device, stripes, new strip, directory, and relative addresses substantially correspond to like named elements recited in Claim 1.

Claim 4

Claim 4 depends from Claim 1 and defines the location of logical tracks in terms of the ID of the stripe and the offset of the track within the stripe. *See* Specification, Figures 3 and 4, page 16, lines 16-18. Consequently, adding a strip to each stripe (through addition of the storage device) does not change the relative address (stripe number, offset) for each strip in the directory. *See* Specification, Figures 3 and 4, page 20, line 21 – page 21, line 2. Adding the strip has changed the logical block address of each block, however, the LSA directory of Claim 4 uses the relative address (stripe number, offset) instead of the logical block address. *Id.*

Claim 6

Claim 6 defines movement of data (D0, D1, D2) and parity strips (P0, P1, P2) during normal operations subsequent to adding the additional storage device (Disk 4). *See* Specification, Figures 3 and 4, page 18, lines 8-15. The algorithm is described in the Specification on page 18, line 17 – page 19, line 5. By following this algorithm the parity strips become rotated to a position the parity strips would have held had the additional storage device been included in the initial building of the array. *See* Specification, page 18, lines 8-15.

Claim 7

Claim 7 defines movement of data (D0, D1, D2) and parity strips (P0, P1, P2) using a background task subsequent to adding the additional storage device (Disk 4). *See* Specification, Figures 3 and 4, page 19, lines 7-22. The present invention provides that the number of moves required to suitably position the parity strips is less than conventional methods. *See* Specification, page 19, lines 17-22.

Claim 8

Claim 8 defines a bitmap used by the controller to implement the movement of data (D0, D1, D2) and parity strips (P0, P1, P2) during normal operations subsequent to adding the additional storage device (Disk 4) as recited in Claim 6. This bitmap is used to temporarily track whether data and parity strips should be moved. Specification on page 18, line 17 – page 19, line 5.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are presented for review on appeal:

I. The rejection under 35 U.S.C. §103(a) of Claims 1-8 and 12-22 as obvious in view of Schultz and Brady.

II. The rejection under 35 U.S.C. §103(a) of Claims 1-22 as obvious in view of Brady and Choy.

7. ARGUMENT

I. The rejection under 35 U.S.C. §103(a) of Claims 1-8 and 12-22 as obvious in view of Schultz and Brady.

The Prior Art. The Schultz and Brady references combined to reject the claims under Section 103 are summarized below.

Schultz. Schultz teaches adding a storage device to a RAID array by moving each stripe to a posting cache and then back to the RAID array configured with the additional storage device. *Schultz* at col. 2, 41-64, col. 3, 4-10, Figs. 2A-2F. Schultz further teaches expansion or contraction of an array of disks in a RAID array. *Schultz* at col. 2, 41-43 ("A disk controller according to the present invention performs on-line reconfiguration of RAID 1, RAID 4 or RAID 5 disk arrays in a hard disk drive system."). Schultz teaches reconfiguration of a RAID array by a process of identifying pre-reconfiguration data as a source logical volume and then reconfiguring the data into a destination logical volume configuration. *Id.* at col. 2, 41-64, col. 3, 4-10, Figs.

2A-2F. Schultz describes in detail the hardware required for a RAID configured disk storage array. *Id.* at col. 3, 66-col. 8, 8, Fig. 1.

Thus, Schultz addresses the problem of adding a storage device to a RAID array while keeping the RAID array on-line, accessible to a host system. Schultz includes no mention of any other storage disk configuration. As noted by the Examiner, there is specifically no mention of a Log Structure Array (LSA). *See* last Office Action mailed April 13, 2004, page 3. In addition, there is no mention of an LSA directory, an LSA sub-directory, a garbage collection system, a bitmap detailing valid and invalid data, or any other hardware or software necessary to make an LSA disk storage system workable with the Schultz invention.

<u>Brady</u>. Brady teaches reducing the memory required for using and managing an LSA directory by creating an LSA subdirectory. *Brady* col. 3, lines 51-56, Abstract. Much like traditional memory cache systems, the LSA subdirectory in Brady includes the logical track addresses of the most recently accessed logical tracks. *Id.* There is no teaching of expansion or contraction of the number of disks in an array.

Of particular note are Brady's teachings regarding mappings within an LSA directory and/or LSA subdirectory between a logical track and a physical location. *Brady* col. 7, lines 21-33. Specifically, Brady teaches that an entry in the LSA directory/subdirectory includes a 6-tuple: a logical track address, a track number within a segment, a segment, a segment column, a starting sector, and a number of sectors. *Brady*, col. 6, lines 49-53. Furthermore, three elements of the 6-tuple are specifically identified as indicating the physical address of a logical track. The three elements include segment number X, segment column Ci, starting sector within a [segment] column Si. *Brady*, col. 7, lines 25-33. This addressing technique is discussed in more detail below.

<u>Prima Facie Obviousness under 35 U.S.C. § 103</u>

<u>All Limitations</u>

"To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." MPEP §2143.03. The Federal Circuit has held that

"the 'subject matter' that must have been obvious to deny patentability under § 103 is the entirety of the claimed invention," *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1576 (Fed. Cir. 1987).

In the present case however, Schultz and Brady fail to disclose the entirety of the claimed invention. Specifically, Schultz and Brady fail to disclose an LSA "directory which specifies storage locations using relative addresses." *Claims*, Claim 1. The relative addressing enables storage devices to be added or removed without affecting the existing entries in the present invention's LSA directory 116.

<u>Motivation to Combine</u>

"It is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor." *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934 (Fed. Cir. 1990) See e.g. *Interconnect Planning Corp. v. Feil,* 774 F.2d 1132, 1143, 227 USPQ 543, 551 (Fed.Cir.1985). To establish *prima facie* obviousness, there must be some suggestion or motivation to modify the reference or to combine reference teachings to arrive at the claimed invention. "The teaching or suggestion to make the claimed combination ... must be found in the prior art, not in applicant's disclosure." MPEP 2143, citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). "The mere fact that references <u>can</u> be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." See *MPEP 2143.01*, citing *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990).

Appellant argues herein that Schultz, Brady, and Choy do not teach or disclose relative addressing, specifically LSA directory addressing that uses an ID of a stripe and the offset, especially, "a construct comprising a stripe number and an offset." *See* Claim 1, and proposed amendment filed July 13, 2004. However, even if Schultz, Brady, and Choy did teach a relative addressing as recited in the claims, Appellant finds no motivation in **the references** to combine Schultz, Brady, and Choy or the desirability of such a combination to arrive at the present invention. The cited Schultz, Brady, and Choy references teach certain claim elements not

related to LSA and expanding RAID arrays, but fail to disclose, suggest, or motivate modifying any of the references to arrive at the present invention ***as a whole***.

Claim 1.

All Limitations

Appellants assert that Schultz and Brady fail to disclose an LSA "directory which specifies storage locations using **relative addresses**." *Claims*, Claim 1. The specification clearly indicates that relative addressing, of which a stripe number and offset is one form, is distinct from Logical Block Addressing (LBA) presently used in the art. *Specification*, page 16, lines 16-19.

LBA.

LBA is an addressing technique used to allow a host to read and write data to addresses (sectors) of a storage device in excess of five-hundred and twenty eight megabytes. *See* included evidence defining logical block addressing. LBA was first introduced to overcome legacy limits of protocols and the like in accessing specific physical locations of large storage devices. Consequently, an LBA facilitates mapping between a specific physical location and a logical address. Therefore, there is a direct relationship between an LBA and a specific location on the storage device. Such a relationship is known in the art as absolute addressing. An absolute address is "an address that directly identifies a storage location without the use of an intermediate reference." *See* included definition of absolute address.

Relative Address.

In contrast to an absolute address, a relative address is a computed address that requires two pieces of information. First, a base address is required. Second, the distance or number of address locations (also known as an offset) from the base address is required. A relative address is "an address that is expressed as a difference in relation to a base address." *See* included evidence definition of relative address. A base address is "an address that is used as the origin in

the calculation of addresses in the execution of a computer program." *See* included evidence definition of base address.

Therefore, an absolute address is the address of the actual physical location on the storage device 106. *See* Figure 1. By way of analogy, an absolute address is comparable to a street address for a residence. Once the street address is provided no additional information is required to locate the physical location.

A relative address represents a physical location using a base address and an offset. Using the same analogy, the same residence can be identified by a relative address such as "the third house from the corner" (assuming at least three houses on one side of the street that includes the corner). Typically, the offset is added or subtracted from the base address. Here the corner is the base address. Moving to the third house represents the offset.

The concept of relative addresses is taught is in relation to a Redundant Array of Inexpensive Disks (RAID) configuration. Specifically, tracks are located using a construct {stripe number, offset}. *See* Specification page 16, lines 16-19. This is a relative address. The stripe number represents the base address and the offset is the distance between the base address and the physical location or absolute address. The benefit of using a relative addressing technique is that few, if any, entries in the LSA need to be altered when a storage device is added or removed from the RAID. *See* Specification page 16, lines 26-29. Because the new storage device includes the same number of stripes, the base address remains the same in each stripe. The difference is that the offset is greater to reach physical locations on the new storage device.

Of course for the offset to properly direct a read/write operation to the proper physical location, the offset must be defined. In one embodiment of the present invention, an LSA segment maps to one RAID stripe, a RAID strip maps to a segment column, and the block offset into a segment is the same as a block offset into a RAID stripe. *See* Specification page 16, lines 22-24. In this manner, use of an offset in the LSA directory enables a read/write operation to add an offset to the base address, the stripe number, to locate the physical address for a specific block.

Appellant respectfully asserts that the addressing used in Brady is absolute addressing and not relative addressing. The Examiner recites a 3-tuple LSA entry used to identify logical tracks. The Examiner asserts: "The values of X, Ci, and Si represents the claimed "relative address."

See Final Office Action, April 13, 2004, page 4. This addressing technique, however, is nothing more than absolute addressing using an address structure having three dimensions, namely a segment number X, a segment column Ci, and a starting sector within a column Si. Together each value is an absolute address, the only difference is that instead of a single dimension address structure, the Brady address structure has three dimensions. By referencing X, Ci, and Si a specific physical storage location is directly identified. *See* definition of absolute address.

Consider, by way of example, a Cartesian coordinate system having an X, Y axis. Any point in the system can be directly identified or addressed using an X,Y pair. The X and Y values are measured with respect to the axis. However, there is no base address and there is no offset. Appellant also finds no base address or offset in Brady.

There is no teaching or suggestion in Brady to add or subtract the X, Ci, and Si. Appellants assert that such teaching is absent because it would contrary to the absolute addressing technique taught in Brady. Therefore, the addressing system of a Cartesian coordinate system is not relative addressing. By direct analogy, the addressing system of Brady that includes segment, segment column, and starting sector is not relative addressing.

The term relative addressing is well known to those of skill in the art and is not confused with direct addressing as used in a Cartesian coordinate system or similarly Brady. Furthermore, the teaching combined with the figures 2-4 provide sufficient teaching and antecedent basis for the term relative addressing. *See* Specification page 16, lines 16-19, Figures 2-4. Appellants respectfully assert that sufficient teaching to define a term that is then used in the claims has been provided. Therefore, Appellant respectfully requests that the antecedent basis rejection of the specification be withdrawn.

Appellant respectfully asserts that Schultz and Brady fail to disclose, singly or in combination, an LSA "directory which specifies storage locations using **relative addresses**." Instead, Brady discloses absolute addressing into an address structure having multiple dimensions. Brady teaches directly addressing the physical locations, there is no base address and no offset. Because this addressing technique renders the present invention unobvious, Appellant asserts that claim 1 is allowable.

Motivation to Combine

The Examiner rejected claim 1 by picking and choosing isolated teachings from the Schultz, Brady, and Choy references and pasting them together to recreate the claims. None of these references suggest nor teach the combination of an LSA controller "which specifies storage locations using relative addresses." (or a construct comprising a stripe number and an offset). *Claims*, Claim 1. Because the Examiner has shown no motivation or suggestion to combine the prior art references relied on in the rejection, Appellant asserts that claim 1 is allowable.

Claims 12, 16 and 20

All Limitations and Motivation to Combine

Claims 12, 16, and 20 defines substantially the same subject matter as Claim 1 and are directed respectively to an apparatus, apparatus, and system. Appellant respectfully asserts that Claims 12, 16, and 20 are allowable for at least the same reasons as Claim 1 with respect to Shultz and Brady.

Claim 4.

All Limitations

Claim 4 depends from claim 1 and should be allowed for all the same reasons stated above regarding claim 1. In addition, claim 4 includes the limitation "...wherein the directory comprises a LSA directory which specifies **the location** of a logical track in terms of the **ID of the stripe** to which the track belongs and **the offset** of the track within the stripe." *Claims*, claim 4, emphasis added. Appellant submits that Claim 4 recites the novel concept of relative addressing in an LSA directory using RAID storage devices. Claim 4 specifically recites the constructs to be used to implement relative addressing: ID of the stripe and the offset.

As discussed above, Schultz and Brady fail to teach or disclose LSA directory entries specifying location using ID of a stripe (stripe number) and an offset. Again, this language is supported in the specification. *See* Specification page 16, lines 16-19, Figures 2-4.

The Examiner rejected Claim 4 initially based on teachings in Brady about LSA directories citing to Brady col. 2, lines 1-7, 30-31. In the Final Office Action, the Examiner cites

to column 7, lines 21-33 and column 8, lines 37-43. However, as indicated above, Appellant finds no teaching in Brady about an offset. The 3-tuple and 6-tuple referred to are multidimensional coordinates of an absolute address. There is no teaching of a base address that would correspond to the ID of the stripe as specifically recited in Claim 4.

"All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). *MPEP* §2143.03. The Federal Circuit has held that "the 'subject matter' that must have been obvious to deny patentability under § 103 is the entirety of the claimed invention," *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561, 1576 (Fed. Cir. 1987). MPEP §2143.03.

The terms **offset** and **ID of the stripe** appear to have received little, if any, consideration from the Examiner. The ID of the stripe and the offset are two aspects that are not taught or disclosed in Brady, Schultz or Choy. Appellant notes that the Examiner cites to Appellant's disclosure to assert that the segment column maps to a RAID stripe and block offset into a segment is the same as a block offset into a RAID stripe. Appellant submits however, that these are teaching of the Appellant and relate to the claimed invention, not teachings of the art. Appellant respectfully directs the Examiner and Board to the Specification page 16, lines 19-20, where these mappings are taught to relate to the "present invention." Therefore, these teachings are unavailable as prior art against Claim 4.

Therefore, the Examiner failed to consider the "entirety of the claimed invention" with respect to Claim 4. Brady and the other art of record fail to teach, disclose, or suggest LSA directory entry addressing using relative addressing with a base address such as ID of the stripe and an offset.

Appellant finds no mention of how or where one of the prior art references teach or disclose the claimed feature of using the ID of the stripe and the offset in LSA directory addressing. As described above, such a distinction is significant as storage devices can be added or removed from the array without affecting the existing LSA directory entries.

Appellants respectfully assert that this oversight by the Examiner has cost the Appellant unnecessary delay and expense in procuring a patent for the claimed invention. Appellants respectfully request that the rejection be reversed.

Furthermore, the Examiner failed to enter an amendment to Claim 1 filed July 13, 2004 that would eliminate any antecedent basis concerns regarding the term "relative addresses." The Claim 1 amendment would have changed "relative addresses" to "a construct comprising a stripe number and an offset." The similarities between the Claim 1 amendment and Claim 4 are clear. Still, the Examiner indicated that the Claim 1 amendment would require further search and/or consideration.

Appellant respectfully disagrees and submits that the subject matter of Claim 4 provided sufficient opportunity to search and consider the idea of a base address and an offset. Appellant anticipates that the explanation of relative addressing discussed above clarifies the novelty found in Claim 4 and the proposed similar amendment to Claim 1.

Appellants submit that the Examiner's failure to give full weight and consideration to the terms in Claim 4 is reversible error.

Motivation to Combine

Neither Schultz, Brady, nor Choy teach or suggest the combination of an LSA controller and "a LSA directory which specifies the location of a logical track in terms of the ID of the stripe to which the track belongs and the offset of the track within the stripe." *Claims*, Claim 4. Because the Examiner has shown no motivation or suggestion to combine the prior art references relied on in the rejection, Appellant asserts that claim 4 is allowable.

Claim 6.

All Limitations

Claim 6 depends indirectly from Claim 1 and should be allowed for all the same reasons stated above regarding claim 1. In addition, Claim 6 includes the limitation "...the data and parity strips are moved to the additional storage device during normal IO operations to the devices." *Claims*, claim 6. The Examiner asserts that Schultz teaches moving of parity strips during normal I/O operations. *See* Final Office Action page 5.

Appellants submit that Schultz teaches adding a storage device to a RAID array by moving each stripe to a posting cache and then back to the RAID array configured with the additional storage device. *Schultz* at col. 2, 41-64, col. 3, 4-10, Figs. 2A-2F. Schultz teaches that

all the stripes are processed together. Furthermore, the phrase "normal IO operations" as it relates to storage devices is well known by those of skill in the art to refer to normal read and write operations. Appellants respectfully submit that exchanging stripes with a posting cache is time consuming and disruptive and is anything but "normal I/O operations" for one or more storage devices under control of an LSA controller.

In contrast, the present invention teaches that a new storage device may be added and parity strips left in place. Then, as part of normal caching and writing of stripes, the parity bits will be written on to the new storage device as though the storage device was in place when the array was originally configured. *See* Specification page 18, line 8 – page 19, line 5. There is no teaching in Schultz that stripes are written as part of a normal destaging process. To the contrary, Schultz teaches that all the stripes are swapped to the cache and then to the new configuration of the array. Such a process is more time consuming than the claimed invention.

Appellants submit that the lack of a prior art reference teaching the features of Claim 6 renders Claim 6 patentably distinct and nonobvious.

<u>Motivation to Combine</u>

Because neither Schultz, Brady, nor Choy teach or suggest the limitation "...the data and parity strips are moved to the additional storage device during normal IO operations to the devices," the references also fail to teach or suggest a motivation or suggestion to combine the prior art references as relied on in the rejection. Appellant asserts that claim 6 is therefore allowable.

<u>Claim 7.</u>

<u>All Limitations</u>

Claim 7 depends indirectly from Claim 1 and should be allowed for all the same reasons stated above regarding claim 1. In addition, Claim 7 teaches that movement of parity strips is performed by a background task. The Examiner cites Schultz in which disk array reconfiguration is a background task. *Schultz* Abstract.

As discussed above, each claim term is to be considered. Here, the Examiner has failed to consider that the "background task is defined by the controller." *Claim* 7. In Schultz, the

whole disk array reconfiguration process is run by firmware. In contrast, in the claimed invention, the background task is a sub-task of the whole process. Therefore, the background task may be conditionally executed separate from the reconfiguration process depending on certain circumstances such as available processing cycles. Therefore, the claimed invention offers more control over when and how the background process is defined and executed. Appellant asserts that claim 7 is allowable because the limitations of claim 7 are not disclosed by Schultz as asserted by the Examiner.

Motivation to Combine

Because neither Schultz, Brady, nor Choy teach or suggest the limitation that movement of parity strips is performed by a background task, the references also fail to teach or suggest a motivation or suggestion to combine the prior art references as relied on in the rejection. Appellant asserts that claim 7 is therefore allowable.

Claim 8.

All Limitations

Claim 8 depends indirectly from Claim 1 and should be allowed for all the same reasons stated above regarding claim 1. In addition, claim 8 teaches a bitmap used to track whether the stripe is in an N+1 or N+2 arrangement. In other words, the bitmap tracks whether parity strips have been moved in a particular stripe to meet the RAID 5 protocol.

The Examiner cites a bitmap in Brady. Brady, col. 8, lines 47-67 and figures 5a-5c. However, the teachings of Brady relate to tracking whether a track in cache has been modified. If so, the version of the track on the storage device is invalid and can be consolidated with others to free up storage space. *See* Brady col. 6, lines 36-45. Such garbage collection tracking is very different from the temporary use of the bitmap in the claimed invention.

The temporary bitmap in claim 8 is used until all stripes have been written with the parity strip in the appropriate position. In contrast, the garbage collection bitmap of Brady must be constantly maintained so that the LSA controlled array functions properly. Appellant asserts that Claim 8 is allowable because the bitmap taught in Brady does not relate to whether a parity strip has been repositioned, if necessary.

Motivation to Combine

Because neither Schultz, Brady, nor Choy teach or suggest the limitation that a bitmap used to track whether the stripe is in an N+1 or N+2 arrangement, the references also fail to teach or suggest a motivation or suggestion to combine the prior art references as relied on in the rejection. Appellant asserts that claim 8 is therefore allowable.

II. **The rejection under 35 U.S.C. §103(a) of Claims 1-22 as obvious in view of Brady and Choy.**

The Prior Art. The Brady reference is summarized above and the Chot reference is summarized below.

Choy. Choy teaches the addition of a storage device to a RAID array by initializing the added storage device to zero, leaving all of the data and parity data in the locations they were in prior to the addition, and remapping a logical device so some parity locations are designated data and the corresponding new strip is re-designated as parity for the associated stripe. *Choy* at col. 5, 14-16, col. 5, 40-col. 6, 21, Fig. 4. The resultant array leaves the designated parity locations in a non-conventional configuration with parity information not uniformly distributed. *Id.* at Fig. 4.

In a second embodiment, Choy teaches swapping data in strips with "intermediate parity storage, as shown by the Pi notation." *Choy* at col. 9, 22-col. 10, 49 (internal quotes deleted), Fig. 7. The resulting parity data is in a configuration corresponding to a RAID array as it would have been with the added storage device present when the array was first configured. *Id.* at Fig. 7. However, the data in the array is out of order and is no longer sequential. *Id.* To provide sequential data an properly distribute the parity, Choy must change the absolute addresses in the mapping instruction both for location reference and for labeling the data as data or parity data.

Prima Facie Obviousness. For the present invention to be obvious, the suggestion to make the invention's combination must be found in the prior art. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). It is "impermissible to use the claims as a frame and the prior art references as a mosaic to piece together a facsimile of the claimed invention." *Uniroyal v.*

Rudkin-Wiley, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988) (citing *W. L. Gore & Associates v. Garlock, Inc.*, 220 USPQ 303, 312). Yet, it appears that is what the Examiner has done, citing references with certain the elements of the present invention but lacking all limitations of the present invention or any suggestion or teaching for the combination.

Appellants respectfully assert that if the prior art of record so clearly demonstrates the obviousness of the claimed invention, a single reference would teach more than just one or two elements of the claimed invention. However, the formation of the combinations used in the rejections is indicative of impermissible hindsight analysis by the Examiner. Furthermore, the Examiner cites to Appellants own teaching in rejecting Appellants claims. *See* Final Office Action page 4. As indicated above, this teaching was provided in reference to the "Present Invention" and not a reference to the current state of the art. Appellants respectfully assert that because such analysis is improper the rejections should be overturned.

<u>Claim 1</u>

Appellant respectfully asserts that the teaching or suggestion to make the claimed combination is only found in the Appellant's disclosure. Neither Schultz nor Brady teach a LSA directory that uses relative addressing, specifically, using a stripe ID and an offset. The present invention provides the only suggestion for LSA array addressing using a stripe ID and an offset. Appellant asserts that claim 1 is allowable because the teaching of an LSA directory that uses a stripe ID and an offset to locate logical tracks is only found in the present invention and not in the prior art relied on in the rejection.

<u>Claims 12, 16 and 20</u>

Claims 12, 16, and 20 defines substantially the same subject matter as Claim 1 and are directed respectively to an apparatus, apparatus, and system. Appellant respectfully asserts that Claims 12, 16, and 20 are allowable for at least the same reasons as Claim 1 with respect to Brady and Choy.

Claim 4.

Neither Schultz or Brady teach the elements defined in Claim 4. Choy also fails to teach or suggest the limitation "...wherein the directory comprises a LSA directory which specifies the location of a logical track in terms of the ID of the stripe to which the track belongs and the offset of the track within the stripe." Therefore, Claim 4 is nonobvious over Schultz, Brady, and Choy.

Claim 6.

Neither Schultz or Brady teach the elements defined in Claim 6. Choy also fails to teach or suggest the limitation "...the data and parity strips are moved to the additional storage device during normal IO operations to the devices." Therefore, Claim 6 is nonobvious over Schultz, Brady, and Choy.

Claim 7.

Neither Schultz or Brady teach the elements defined in Claim 7. Choy also fails to teach or suggest the limitation that movement of parity strips is performed by a background task. Therefore, Claim 7 is nonobvious over Schultz, Brady, and Choy.

Claim 8.

Neither Schultz or Brady teach the elements defined in Claim 8. Choy also fails to teach or suggest the limitation that a bitmap used to track whether the stripe is in an N+1 or N+2 arrangement. Therefore, Claim 8 is nonobvious over Schultz, Brady, and Choy.

No Prima Facie Obviousness Established.

In view of the foregoing, the Examiner has not properly established *prima facie* obviousness rejections of Claims 1-8 and 12-22 or Claims 1-22. Appellant respectfully requests reversal of the 35 U.S.C §103 rejections and allowance of Claims 1-8 and 12-22 or Claims 1-22. Appellant submits that the foregoing arguments further establish the non-obviousness of the present invention. Reversal of the rejections and allowance of the pending claims is respectfully requested.

8. CLAIMS APPENDIX

1. (Previously Amended) A method of adding an information storage device to a plurality of information storage devices in an information processing system in which a processor is connected for communication with the information storage devices by means of a log structured array (LSA) controller in which the information is stored as a plurality of stripes extending across the devices of the array, the LSA controller further defining a directory which specifies storage locations using relative addresses, the method comprising connecting the additional information storage device to the LSA controller and logically appending an additional strip provided to each existing stripe by the additional storage device to the end of each stripe in the directory.

2. (Original) The method of claim 1, further comprising configuring the plurality of information storage devices as an N+1 array.

3. (Original) The method of claim 1, wherein each stripe comprises N information strips and one parity strip, each information strip storing an integer number of logical tracks.

4. (Previously Amended) The method of claim 1, wherein the directory comprises a LSA directory which specifies the location of a logical track in terms of the ID of the stripe to which the track belongs and the offset of the track within the stripe.

5. (Previously Amended) The method of claim 1, wherein prior to the addition of the additional storage device, the parity strips are rotated amongst the N+1 information storage devices in accordance with a RAID-5 architecture, the method further comprising moving selected parity strips to the additional information storage device at locations that would have stored parity strips had the array originally comprised N+2 information storage devices.

6. (Original) The method of claim 5, wherein the data and parity strips are moved to the additional storage device during normal IO operations to the devices.

7. (Original) The method of claim 5, wherein a background task is defined by the controller to move the data and parity strips to the additional storage device.

8. (Previously Amended) The method of claim 6, wherein a bitmap is defined by the controller, each bit of the bitmap representing an array stripe and indicating whether the data and parity strips of the stripe are located in their original position or in the position appropriate to the plurality of information storage devices including the additional information storage device .

9. (Original) The method of claim 1, wherein the additional information storage device is initialised to all binary zeros prior to connection to the controller.

10. (Original) The method of claim 1, further comprising connecting a plurality of additional information storage devices to the log-structured array controller and logically appending the additional strips, provided to each existing stripe by the additional storage devices, to the end of each stripe in the LSA directory.

11. (Previously Amended) The method of claim 1, wherein connecting the additional information storage device to the LSA controller further comprises:

initializing the new disk to all binary zeroes so that the new disk can be included in the parity calculations without modifying the parity already on disk;

temporarily suspending accesses to a RAID 5 array controlled by the LSA controller and flushing any data cached by the RAID array prior to temporarily suspending access;

adding the new disk as a member of the RAID array; and

applying an algorithm to optionally relocate the parity and/or the data.

12. (Previously Amended) A log structured array (LSA) controller comprising a logic device configured to control the transfer of information between a processor and a plurality of information storage devices in which the information is stored as a plurality of stripes extending across the devices of the array, and further configured upon the addition of a new information storage device to the array, to logically append to the end of each stripe in a directory a new strip

provided for the new information storage device, the directory specifying storage locations using relative addresses.

13. (Original) The LSA controller of Claim 12, wherein the plurality of information storage devices are configured as an N+1 array.

14. (Original) The LSA controller of Claim 12, wherein each stripe comprises N information strips and one parity strip, each information strip storing an integer number of logical tracks.

15. (Previously Amended) The LSA controller of Claim 12, wherein the directory further comprises an LSA directory specifying the location of a logical track in terms of the ID of the stripe to which the track belongs and the offset of the track within the stripe.

16. (Previously Amended) A log structured array (LSA) controller for adding an information storage device to a plurality of information storage devices in an information processing system in which a processor is connected for communication with the information storage devices by means of a log structured array (LSA) controller in which the information is stored as a plurality of stripes extending across the devices of the array, the LSA controller comprising:

a directory which specifies storage locations using relative addresses;

means for connecting the additional information storage device to the LSA controller; and means for logically appending an additional strip provided to each existing stripe by the additional storage device to the end of each stripe in the directory.

17. (Previously Amended) The log structured array (LSA) controller of claim 16, further comprising means for configuring the plurality of information storage devices as an N+1 array.

18. (Previously Amended) The log structured array (LSA) controller of claim 16, wherein each stripe comprises N information strips and one parity strip, each information strip storing an integer number of logical tracks.

19. (Previously Amended) The log structured array (LSA) controller of claim 16, wherein the directory comprises a LSA directory which specifies the location of a logical track in terms of the ID of the stripe to which the track belongs and the offset of the track within the stripe.

20. (Previously Amended) An information storage system comprising:

a plurality of information storage devices;

a processor connected for communication with the information storage devices by means of a log structured array (LSA) controller in which the information is stored as a plurality of stripes extending across the devices of the array,

an LSA controller comprising a directory which specifies storage locations using relative addresses, the LSA controller configured to connect an additional information storage device to the LSA controller and logically append an additional strip provided to each existing stripe by the additional storage device to the end of each stripe in the directory.

21. (Original) The information storage system of claim 20, wherein the plurality of information storage devices comprise an N+1 array.

22. (Original) The information storage system of claim 20, wherein each stripe comprises N information strips and one parity strip, each information strip storing an integer number of logical tracks.

9. EVIDENCE APPENDIX

In compliance with CFR §41.12 the non-binding authorities relied upon above are cited below. Copies of these references are also included.

Internet word search on the website at URL http:// searchsmallbizit.techtarget.com /gDefinition/0,294236,sid44_gci214074,00.html for the term "logical block addressing"

Internet website located at URL http://www.atis.org/tg2k/_absolute_address.html
Internet website located at URL http://www.atis.org/tg2k/_relative_address.html
Internet website located at URL http://www.atis.org/tg2k/_base_address.html

10. RELATED PROCEEDINGS APPENDIX

There are no related proceedings.

SUMMARY

In view of the foregoing, each of the claims on appeal has been improperly rejected. Reversal of the Examiner's rejection and allowance of the pending claims 1-22 is respectfully requested.

Respectfully submitted,

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logical block addressing

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Logical block addressing is a technique that allows a computer to address a hard disk larger than 528 megabytes. A logical block address is a 28-bit value that maps to a specific cylinder-head-sector address on the disk. 28 bits allows sufficient variation to specify addresses on a hard disk up to 8.4 gigabytes in data storage capacity. Logical block addressing is one of the defining features of Enhanced IDE (EIDE), a hard disk interface to the computer bus or data paths.

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absolute address: In communications, computer, and data processing systems, an address that directly identifies a storage location without the use of an intermediate reference, *e.g.*, a base address or a relative address. [After Weik '96]

These definitions were prepared by ATIS Committee T1A1. For more information on the work related to these definitions, please visit the ATIS website.

This HTML version of Telecom Glossary 2K was last generated on February 28, 2001. References can be found in the Foreword.

relative address

relative address: In computer and data processing programming, an address that is expressed as a difference in relation to a base address. [After Weik '96]

This HTML version of Telecom Glossary 2K was last generated on Wed Feb 28 15:39:21 MST 2001. References can be found in the Foreword.

base address: 1. An address that is used as the origin in the calculation of addresses in the execution of a computer program. [From Weik '96] **2.** A given address from which an absolute address is derived by combination with a relative address. *Note:* Base addresses are primarily used by computer programmers rather than by computer users. [From Weik '96]